IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method for providing a horizontal scan control signal ~~(SLS)~~ for a TV set from a horizontal synchronization signal ~~(SHS)~~ contained in a composite video signal ~~(CVBS)~~, the horizontal synchronization signal ~~(SHS)~~ containing horizontal synchronization pulses ~~(39)~~ and parasitic pulses ~~(40)~~, said scan control signal ~~(SLS)~~ being provided from an oscillating signal ~~(SO)~~ generated by an oscillator ~~(26)~~ of a phase-locked loop ~~(20)~~ receiving the horizontal synchronization signal ~~(SHS)~~, said oscillating signal ~~(SO)~~ having a frequency depending on a driving signal ~~(SC)~~ provided from the comparison between the horizontal synchronization signal ~~(SHS)~~ and a binary phase signal ~~(PH, PH')~~, wherein, at each parasitic pulse ~~(39)~~ among successive parasitic pulses between two synchronization pulses ~~(40)~~, the driving signal ~~(SC)~~ is successively varied in the increasing direction or in the decreasing direction.

2. (Original) The method of claim 1, wherein the parasitic pulses have variable durations.

3. (Currently Amended) A circuit for providing a horizontal scan control signal ~~(SLS)~~ for a TV set from a horizontal synchronization signal ~~(SHS)~~ contained in the composite video signal ~~(CVBS)~~, the horizontal synchronization signal ~~(SHS)~~ containing horizontal synchronization pulses ~~(39)~~ and parasitic pulses ~~(40)~~, said circuit comprising a phase-locked loop ~~(20)~~ receiving the horizontal synchronization signal ~~(SHS)~~ comprising an oscillator ~~(26)~~ generating an oscillating signal ~~(SO)~~ from which is provided the scan control signal ~~(SLS)~~, the frequency of the oscillating circuit ~~(SO)~~ depending on a driving signal ~~(SC)~~ provided from the horizontal synchronization signal ~~(SHS)~~, and comprising a means ~~(50, 22, 24)~~ for correcting the driving signal ~~(SC)~~ which, at each parasitic pulse ~~(40)~~ among successive parasitic pulses between two synchronization pulses ~~(39)~~, alternately varies the driving signal ~~(SC)~~ in the increasing or

decreasing direction.

4. (Currently Amended) The method of claim 3, further comprising:

a comparator ~~(22)~~ for comparing the horizontal synchronization signal ~~(SHS)~~ and a modified phase signal ~~(PH')~~ and providing, according to the comparison, a current ~~(IPLL)~~ of zero amplitude or of constant amplitude and of variable sign;

a capacitor ~~(24) run through by~~ conducting the current ~~(IPLL)~~ and providing the driving signal ~~(SC)~~; and

a correction circuit ~~(50)~~ providing the comparator ~~(24)~~ with the modified phase signal ~~(PH')~~ corresponding to a binary phase signal ~~(PH)~~ having a frequency proportional to the frequency of the oscillating signal ~~(SO)~~ or corresponding to a binary correction signal ~~(SQ)~~, the state of which switches for each parasitic pulse ~~(40)~~.

5. (Currently Amended) The circuit of claim 4, wherein the correction circuit ~~(50)~~ comprises a switch ~~(55)~~ adapted to alternately connecting, according to a switch control signal ~~(SIC)~~, an output terminal ~~(52)~~ connected to the comparator ~~(22)~~ at a first input terminal ~~(51)~~ receiving the phase signal ~~(PH)~~ or at a second input terminal receiving the correction signal ~~(SQ)~~, the switch signal ~~(SIC)~~ being provided from a binary signal at a first state at the level of a synchronization pulse ~~(39)~~ and at a second state otherwise.

6. (Currently Amended) The circuit of claim 5, wherein the switch signal ~~(SIC)~~ is also provided from at least one binary validation signal ~~(SM, SSTAND, SPLLV)~~ at a first state when a validation condition is fulfilled and at a second state when the validation condition is not fulfilled.

7. (Currently Amended) The circuit of claim 4, comprising a latch ~~(54)~~ providing the correction signal ~~(SQ)~~ receiving a binary latch control signal ~~(SLC)~~ provided from the horizontal synchronization signal ~~(SHS)~~, the state of the correction signal ~~(SQ)~~ switching at each falling edge of the latch control signal ~~(SLC)~~.

8. (Currently Amended) The circuit of claim 7, comprising a filter ~~(53)~~ receiving the horizontal synchronization signal ~~(SHS)~~ and providing the latch control signal ~~(SLC)~~, the latch control signal ~~(SLC)~~ comprising pulses, each pulse being associated with a parasitic pulse ~~(40)~~.